OKI.217D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Hidenori Hasegawa — Group Art Unit: Unknown

Divisional of Serial No.: 09/788,664 — Examiner: Unknown

Filed: JuLY 24, 2003

FOR: SUBSTRATE FOR MOUNTING A SEMICONDUCTOR CHIP AND METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

DRAWING CORRECTION APPROVAL REQUEST

U.S. Patent and Trademark Office
2011 South Clark Place
Customer Window, **Mail Stop Patent Application**
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

Date: July 24, 2003

Sir:

Applicant respectfully requests the Examiner's approval of the following drawing corrections indicated in red ink on the attached sheet.

Fig. 2 has been renumbered separately to include Figures 2(E)-2(G), and the cross sectional lines have been designated properly.

Figs. 6(A)-6(C) have been denoted as "PRIOR ART".

These drawing corrections have been incorporated into the formal drawings filed along with the present application, to expedite prosecution of this application.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.

Andrew J. Telesz, Jr.
Registration No. 33,581

AJT:dmc

12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

Enclosures: Two (2) sheets of red-inked drawings